The Designing of Ionospheric Coherent Beacon Receiver

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ABSTRACT

The designing of ionospheric coherent beacon receiver (ICBR) is based on the subject "Research on the combination of space and ground observation and data fusion technique". Due to the need of signal receiving and measuring accuracy of ionospheric parameters, the design, demonstration and analysis of signal receiving system, antenna designing, front-end designing and intermediate frequency process for ICBR have been fulfilled successfully.

Beacon signals transmitted by low earth orbit satellites can be captured and locked automatically so as to output the amplitude and phase information in real time. Special attention has been paid toovercome many problems such as the receiving of high sensitivity, accuracy and multi-frequency satellite beacon signal.

System composition

The system composition diagram of ICBR can be seen in Figure 1. VHF, UHF and L band signals transmitted by simulator are received through tri-band antenna. Data will finally be sent to data processing center through network after tracking process in receiver and further process in data processing and monitoring terminal.

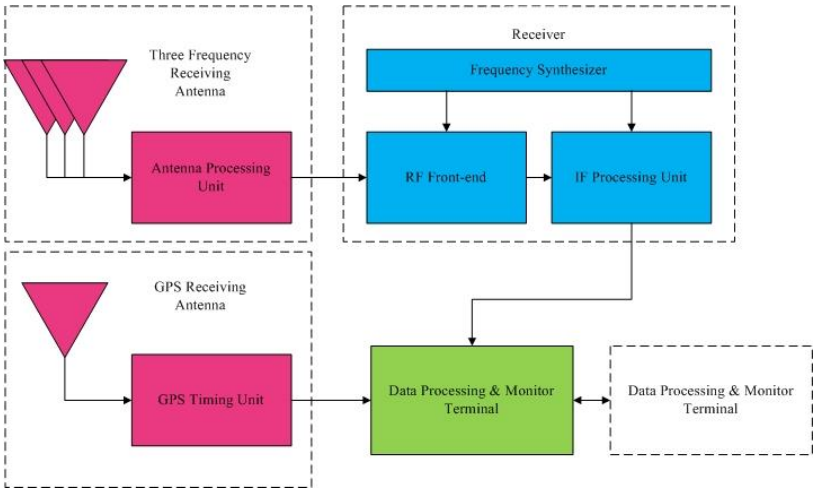

Figure 1. The diagram of system composition

Design of intermediate frequency module

Intermediate frequency processing unit converts analog signal to digital signal and processes relative algorithm and protocol, so it can be called as the carrier of coherent signal algorithm. The hardware structure diagram is shown in Figure 2. Through signal processing circuit, intermediate signals of 1.7MHz output by front-end are then sent A/D converter chip for 3-channel A/D synchronized sampling. The sampling signalsare the input of FPGA to implement synchronized

filter, speed reduction and coherent process. Further steps will be carried out in DSP chip and final results will be sent to the computer by relative protocols in real time. To improve the compatibility of this system, final results can be transmitted to computer either by COM port RS 232 or by network port. The important thing for this intermediate frequency module is the choose of A/D chip, especially the A/D sampling rate and significant digit so as to meet the need of 3-channel phase synchronization.

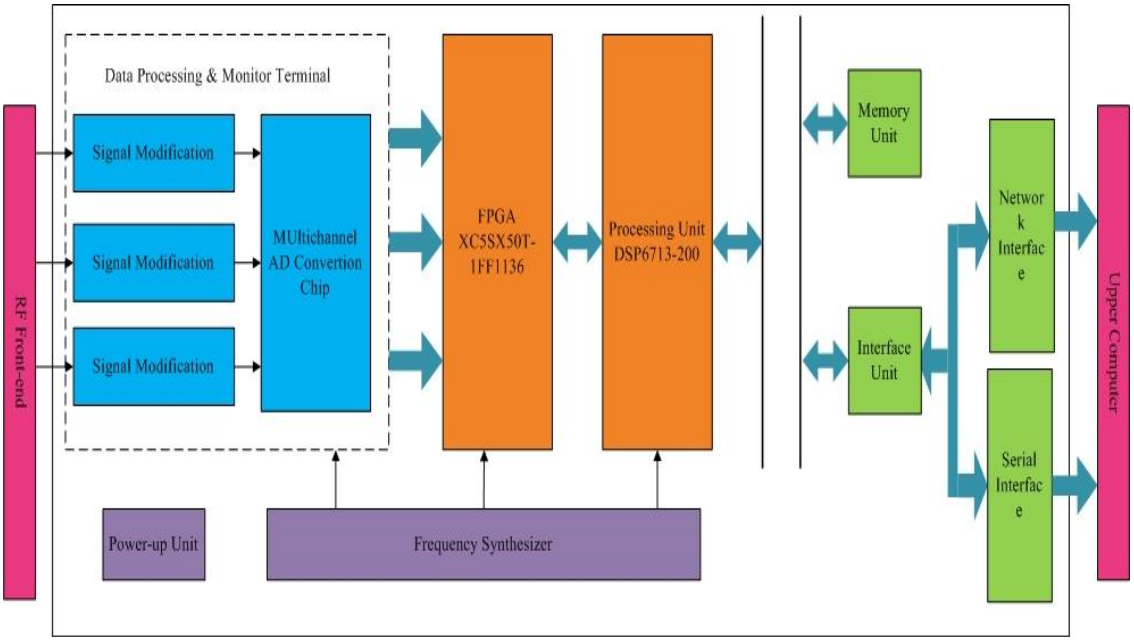

Figure 2. The diagram of hardware structure

Data Process

After locking tri-band beacon signals, the receiver will output the processing results by 50 Hz sampling rate in real time. Total Electron Content (TEC) will be calculated in every second. Phase scintillation index and amplitude scintillation index will be calculated in every 20 seconds respectively. Moreover, the elevation and azimuth of each observation link can be calculated from the information of satellite orbits and position of monitoring stations.